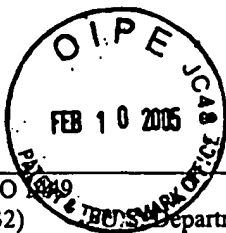
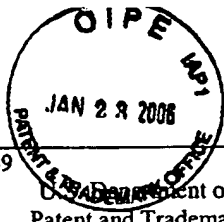


Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office				Atty. Docket No. IMPJ-0027B		Serial No.: Unassigned 10/814866	
Information Disclosure Statement by Applicant				Applicant: Christopher J. Diorio et al.			
(Use several sheets if necessary)				Filed: Herewith Group: Unassigned 3/30/04 2816			
U.S. Patent Documents							
Init.	A	Document No.	Date	Name	Class	Subclass	Filing Date
TH	A	5,761,121	6/2/1998	Chang	365	185.14	10/31/1996
TH	B	5,825,063	10/20/1998	Diorio et al.	257	316	7/26/1996
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TH	D	5,898,613	4/27/1999	Diorio et al.	365	185.03	6/25/1997
TH	E	5,914,894	6/22/1999	Diorio et al.	365	185.03	6/1/1998
TH	F	5,986,927	11/16/1999	Minch et al.	365	185.01	11/10/1998
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TH	M	6,661,278	12/9/2003	Gilliland	327	536	7/8/2002
TH	N	6,664,909	12/16/2003	Hyde et al.	341	144	8/13/2001
Foreign Documents							
							Translation
Init.		Document No.	Date	Country	Class	Subclass	Yes No
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
TH	O	Raszka, Jaroslav, et al., "Embedded Flash Memory for Security Applications in a 0.13µm CMOS Logic Process", IEEE 2004 International Solid-State Circuits Conference, February 16, 2004, pp. 46-47.					
Examiner					Date Considered 11/23/06		
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Form PTO (Rev. 2-32)				Atty. Docket No. IMPJ-0027B		Serial No. 10/814,866		
Department of Commerce Patent and Trademark Office				Applicant: Christopher J. Diorio et al.				
Information Disclosure Statement by Applicant				Filed: March 30, 2004		Group: 2818 2816		
(Use several sheets if necessary)								
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Init.		Document No.	Date	Name	Class	Subclass	Filing Date	
TH	A	2003/0206437	11/6/2003	Diorio et al.	365	185.21	9/16/02	
TH	B	2004/0004861	1/5/2004	Srinivas et al.	365	185.21	7/5/02	
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TH	P	6,384,451	5/7/2002	Caywood	257	321	3/9/00	
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Init.		Document No.	Date	Country	Class	Subclass	Yes	No
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TH	Q	Invitation to Pay Additional Fees (Partial International Search), Application No. PCT/US 03/31792, date of mailing April 22, 2004.						
TH	R	Witters, et al., "Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits", IEEE Journal of Solid-State Circuits, VOL. 24, No. 5, October 1989, pp. 1372-1380.						
Examiner					Date Considered			
Thomas J. Hefner					1/23/06			
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U.S. Department of Commerce Patent and Trademark Office				Applicant: Christopher J. Diorio et al.				
Information Disclosure Statement by Applicant				Filed: March 30, 2004		Group: 2818		
(Use several sheets if necessary)								
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Init.		Document No.	Date	Name	Class	Subclass	Filing Date	
TH	A	4,158,239	1/12/1979	Bertin	365	182	12/20/77	
TH	B	4,541,073	9/10/1985	Brice et al.	365	156	9/28/82	
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TH	Q	6,946,892	9/20/2005	Mitarashi	327	333	01/02/04	
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							Translation	
Init.		Document No.	Date	Country	Class	Subclass	Yes	No
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)								
TH	R	Declercq et al., "Design and Optimization of High-Voltage CMOS Devices Compatible With a Standard 5 V CMOS Technology", IEEE Custom Integrated Circuits Conference, 1993, pp. 24.6.1-24.6.4.						
TH	S	Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique", IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 3, June 1976, pp. 374-378.						
TH	T	International Search Report for PCT/US 03/31792 date mailed August 12, 2004.						
Examiner					Date Considered			
					02/02/06			
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